REMARKS

Claims 22-32 were presented for examination. Claim 22, 23 and 32 were amended. Claims 22-32 are presently pending before the Examiner. Further examination and reconsideration are respectfully requested in view of the amendments and remarks made in this Response.

The Examiner indicated that the current status of the cross-referenced patent applications should be added to the specification. Accordingly, the specification has been amended to indicate the current status of the cross-referenced patent applications.

The Examiner required that a new title, clearly indicative of the claimed invention, be supplied. Accordingly, the title has been amended to clearly indicate the invention to which the claims are directed.

Claims 22-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over S3 Incorporated, S3 Burst Mode DRAM" ("S3 Incorp.") in view of Johnson *et al.* (U.S. Patent 4,581,990; hereinafter "Johnson") or Manning (U.S. Patent 5,610,864; hereinafter "Manning").

The Examiner contends that S3 Incorp. describes a memory with a temporary storage circuit for receiving a first external address referring to a row address in the timing diagrams of Figs. 3 and 4; describes a multiplexer coupled to the temporary storage referring to page 1, left column; and describes mode selection by the memory controller referring to page 1, left column in the introduction section.

The Examiner further states that S3 Incorp. does not specifically disclose mode control logic or a pipelined mode. With respect to the former deficiency, the Examiner states that it is well known in the art to combine mode control logic and a memory circuit into one chip to increase speed, decrease size, and decrease noise. With respect to the latter deficiency, the Examiner contends that Johnson discloses the concept of selecting between a burst mode and a pipelined mode of operation, referring to Johnson at figures 5 and 6, and at column 10, lines 48-49. Alternatively, the Examiner contends that Manning discloses mode circuitry configured to select between two modes, referring to Manning at figure 1, column 5, lines 41-50, and column 6, lines 14-16.

S3 Incorp. is a two page preliminary product overview of a DRAM having a "hyper page mode" (also know as extended data out mode) and a burst mode. In S3 Incorp., pinout diagrams, as well as read and write timing diagrams for each mode, are provided. Notably, the S3 Incorp. product overview provides no schematic diagrams and no block diagrams, other than the above-mentioned pinout diagrams.

Claim 22 recites:

> A memory circuit comprising:
>
> *control logic for providing a selected mode control signal;*
>
> *selection and temporary storage circuitry* for receiving and storing a first external address; and
>
> *a multiplexer coupled to the selection and temporary storage circuitry and to the control logic for receiving* the first external address and *the selected mode control signal* respectively therefrom and for *switching the memory circuit between a burst mode and a pipelined mode*. (Emphasis added.)

It is Applicants' position that S3 Incorp. does not describe or show "selection and temporary storage circuitry" coupled to a "multiplexer" as recited in Claim 22. It is Applicants' position that a memory controller that selects a mode does not describe, show or suggest "control logic for providing a selected mode control signal" to "a multiplexer" as recited in Claim 22. An external mode select signal is recited in dependent Claim 23. Amended Claim 23 recites:

> A memory circuit, as in Claim 22, wherein *the control logic is adapted to receive an external mode select signal* for selecting the burst mode or the pipelined mode and *for determining the selected mode control signal*. (Emphasis added.)

Johnson discloses a RISC processor 101 connected to a data store 103 via shared address bus 111 and data bus 120. (*See*, Johnson, FIG. 1.) The "interface," provided by three separate buses (*see,* Johnson, col.2, lines 38-46), is synchronous (*see,* Johnson, col.8, lines 28-31). In Johnson, an inquiry is made to determine if a memory supports a burst mode or a pipelined mode. (*See*, Johnson, col. 10, lines 48-65.) It is Applicants' position that Johnson does not describe, show or suggest a memory having both burst and pipelined modes; rather, Johnson describes that an inquiry is to be made to determine which type of memory architecture is used, namely, burst or pipelined.

The Examiner contends that Manning discloses mode circuitry configured to select between two modes, referring to Manning at figure 1, column 5, lines 41-50, and column 6, lines 14-16. Manning discloses an asynchronous DRAM having dual modes of operation, namely, burst and EDO page mode (Manning, col. 6, lines 22-26); standard fast page mode and burst mode (Manning, col. 7, lines 43-48); and fast page mode, EDO page mode, static column mode and burst operation (Manning, col. 7, lines 49-54). Though Manning does discuss pipelined architectures (*see,* Manning, col.5, lines 43-50), Manning does not describe, show or suggest a memory having both a pipelined architecture and a burst architecture.

In contrast to Johnson and Manning, the present invention provides a memory circuit that may be switched "between a burst mode and a pipelined mode", as recited in Claim 22. Accordingly, it is respectfully submitted that Claim 22 is allowable over S3 Incorp. in view of Johnson or Manning. With respect to Claims 23-32, they depend from allowable Claim 22, and thus are likewise allowable.

With respect to Claims 23, the Examiner states that S3 Incorp. further suggests an external mode select signal that may be used for selecting between burst mode or page mode. In contrast to S3 Incorp., an external mode select signal of amended Claim 23 is for selecting between a pipelined mode and a burst mode and for determining a selected mode control signal.

With respect to Claim 24, though S3 Incorp. suggests an enable signal, it does not describe, show or suggest mode circuitry coupled to an enable signal for determining a selected mode control signal as claimed.

With respect to Claim 26, the Examiner states that S3 Incorp. discloses a counter. S3 Incorp. recites in relevant part: "...in burst mode, subsequent transfers are generated by sequencing the column address using an internal counter incremented by each CAS cycle." S3 Incorp. does not describe, show or suggest a counter coupled to selection and temporary storage circuitry as claimed in Claim 26.

Claims 28-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over S3 Incorp. in view of Johnson or Manning and further in view of Micron Technology, Inc., "1995 DRAM Data Book," pages 4-1 through 4-42 (hereinafter "Micron"). The above-mention remarks with respect to the rejection of Claims 22-27 are incorporated herein by reference to the rejection of Claims 28-32. As Claims 28-32 depend on independently allowable Claims 22 and 26, Claims 28-32 are likewise allowable.

With respect to Claim 32, the Examiner states that "Johnson discloses a system clock coupled to the processor...the memory not operating directly off the system clock..." The Examiner quotes Johnson, column 10, lines 50-54, which states:

> "If not, a simple access is completed (block 304) with the result and *IRDY or *DRDY being driven over the interface by the slave device. The processor latches the result (block 305), and the simple access is complete."

From which, the Examiner concludes that Johnson "reads on" asynchronous memory operation.

It is Applicants' position that Johnson does not describe, show or suggest asynchronous memory operation.

In Johnson, a timing diagram is provided for each of the following types of memory access: "instruction read - simple access" (*see,* Johnson, FIG. 4), "instruction read - pipelined access" (*see,* Johnson, FIG. 5), and "instruction read - establishing burst mode access" (*see,* Johnson, FIG. 6). In each timing diagram in Johnson, a system clock signal ("SYS CLK" or "SYSCLK") is shown along with the *IRDY

signal, and the *IRDY signal is synchronized to the SYSCLK signal. Johnson defines the *IRDY signal as an instruction ready signal to a processor to indicate that a valid instruction is on instruction bus 115. (*See,* Johnson, col.6, lines 22-25.) Accordingly, the *IRDY signal is provided to a processor in a synchronous manner with respect to the SYSCLK signal.

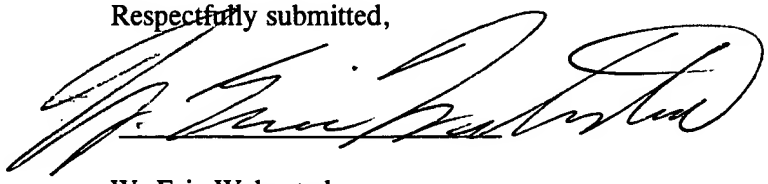
Johnson defines the *DRDY signal as a data ready signal to a processor indicating valid data is on data bus 120 for loads (*i.e.,* a completed read) and indicating an access is complete for stores (*i.e.,* data need not be driven on data bus 120 any longer). (*See,* Johnson, col.7, lines 22-27.) The *DRDY signal only indicates that an access is complete, not that the information is accessed in a synchronous or asynchronous manner.

In sum, the *IRDY signal is described with reference to SYSCLK, and the *DRDY signal provides no insight as to whether an access is synchronous or asynchronous. Thus, it is respectfully submitted that Johnson does not describe, show or suggest an asynchronously-accessible memory operation, rather it discloses a synchronous interface with a burst or pipelined mode command inquiry to a "data store 103." In contrast to Johnson, amended Claim 32 recites:

> A memory circuit, as in Claim 26, wherein the memory circuit is incorporated in an *asynchronously-accessible random access memory*. (Emphasis added.)

For the above-reasons, it is believed that Claims 22-32, all the pending claims, are allowable. As it is believed that the application is in condition for allowance, such allowance is earnestly solicited.

Respectfully submitted,



W. Eric Webostad,
Registration No.35,406,
Patent Counsel,
Micron Technology, Inc.
Mail Stop 525
P. O. Box 6
Boise, ID 83706-9632
(208) 368-4792